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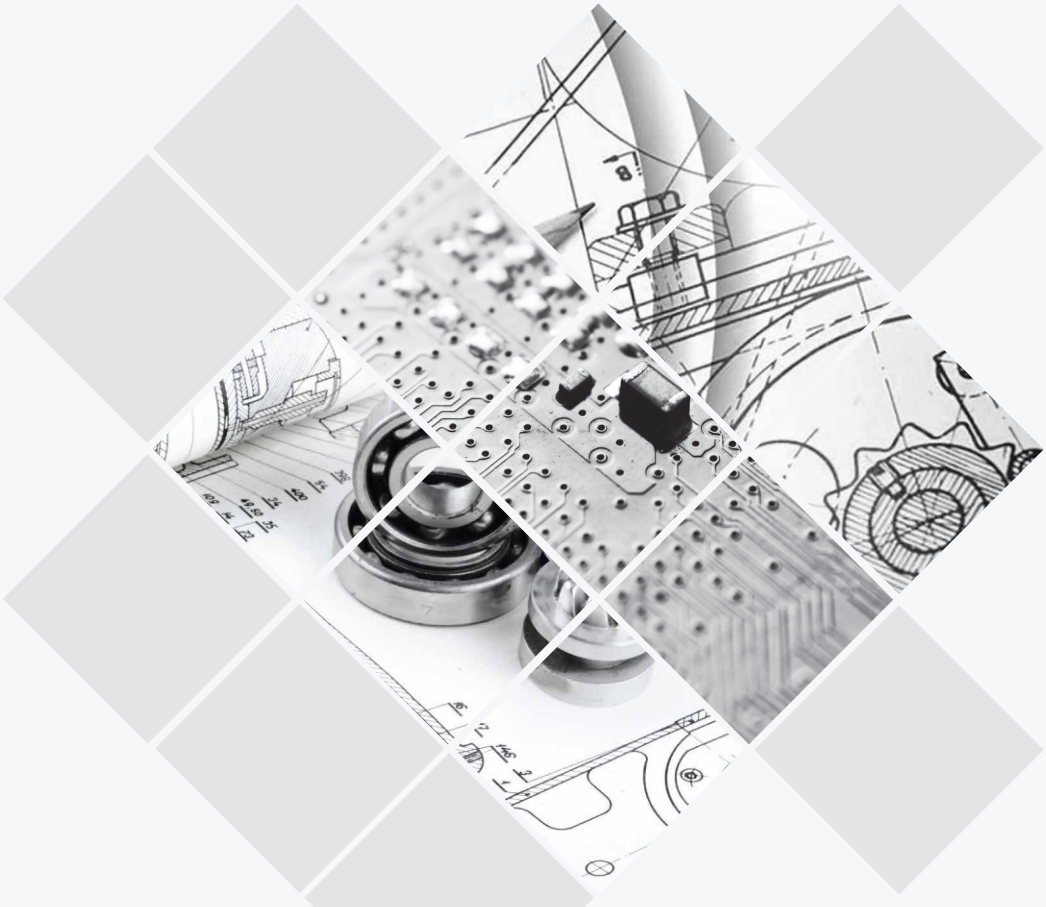
advanced driver assistance system using FPGA

Advanced Driver Assistance System (ADAS) is the front runner of innovations to make driving experience easier and safer on our more congested roads. According to the research firm, Strategy Analytics, ADAS deployment will grow around 10% within next couple of years. The challenges involved in the design of an ADAS processing platforms are power reduction, transportation of video data over high-speed serial interfaces, parallel/serial process partitioning, meeting platform scalability requirement, meeting external memory bandwidth requirement, architectural flexibility and need for on-chip memory resources. This white paper discusses how the processing power of Field Programmable Gate Arrays (FPGAs) and Programmable SoCs can be used to keep pace with consumer innovations.



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contents

Advanced Driver Assistance System using FPGA

Introduction

Automotive industry can't treat safety as an afterthought. Innovations like the airbag, anti-lock braking systems (ABS) and electronic stability programs (ESP) have helped to reduce the number of traffic fatalities and severity of accidents. But increase in the number of vehicles on the road, more than these technologies are needed to address a further reduction of accidents and fatalities. In the last few years Advanced Driver Assistance System (ADAS) features like radar- or camera-based systems have been introduced to make driving safer. ADAS constantly keep an eye on the road and makes sure to alert the driver in real-time of an impending danger. The increased use of complex automotive electronics systems requires that they should be designed for ultra-reliability because the failure of an automotive system could place the vehicle's passengers in a life-threatening situation.

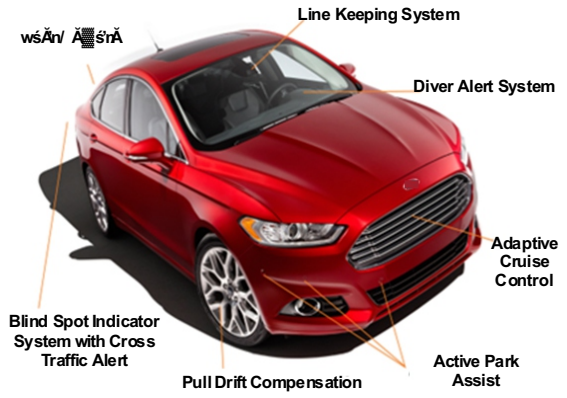


Figure 1 : ADAS features

How is the market evolving?

Government legislation and strong consumer interest in safety features is one of the driving factors contributing to the ADAS market growth. Increased safety awareness and the desire for more driving comfort on the consumer side targets market to grow at a CAGR of 22.59[(1)] percent over the period 2012-2016.
Innovations in remote sensors and associated processing algorithms that extract and interpret critical information also fuel an increase in DA system deployment.

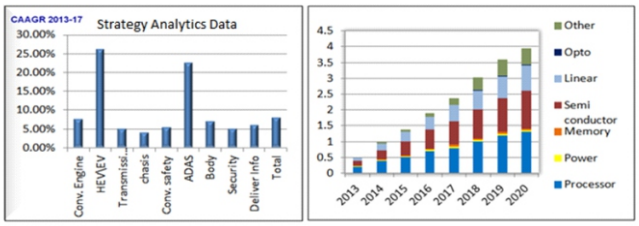


Figure 2: Market Analysis Data(1)

In recent years, the Global ADAS market has also been witnessing the increasing deployment of ADAS in low-cost cars. So the market is on the threshold of enormous growth. In the race to develop reliable and cost-effective ADAS, designers are presented with challenges to integrate functionality, develop scalable platforms and design systems that are robust enough to work in various operating conditions. In order to process multiple algorithms simultaneously, develop a scalable architecture, and get to market on time, ADAS system designers are increasingly turning to FPGAs and PSoCs to solve their challenging problems. The architecture of PSoCs or FPGAs is ideally suited for vision processing applications that require both fine grained parallelism and high-level processing. Automakers and suppliers benefit from IP (intellectual property) and other development aids available to help accelerate time-to-market and reprogram products to meet changing requirements and specifications.

What are the challenges and opportunities?

ADAS are expensive and this could pose a challenge to the growth of this market(5). Suppliers failed to offer extensions to the mandated technology that the consumer will continue to pay extra for. Suppliers need to offer a scalable platform that allows cost-effective deployment with the time to market and low risk in mind. Intellectual Properties used must be certified to the appropriate automotive safety integrity level. To comply with ISO 26262[3], an ADAS supplier must establish procedures associated with safety standards. The industry lacks interoperability specifications for radar, laser, and video data in the car network. Also lacks standards for embedded vision-processing algorithms. ADAS cannot add to driver distraction.

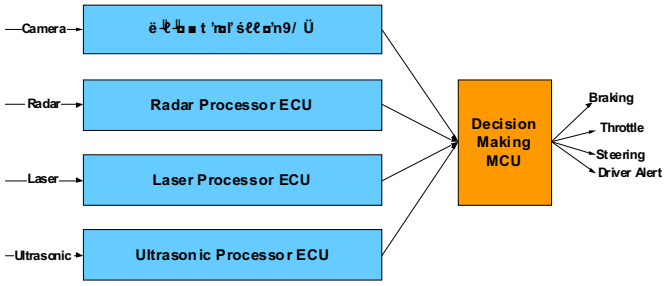
Power dissipation[3] is a crucial parameter since systems are either located behind the windshield in front of the rear-view mirror with direct exposure to sunlight or in the bumper in front of the radiator hence cannot dissipate much heat. Data transactions on external DDR memory especially can consume a substantial amount of power.

Performance and power requirements can be a challenge when using general-purpose CPU architectures with often many cores running at high frequency. In addition, the algorithms used to process video and radar data combined with other data sources makes it difficult for automotive suppliers to determine fixed high-performance architecture.

In order to handle the increased performance requirement, either the image resolution needs to be decreased, or the frame rate reduced or multiple devices need to be used. Therefore ability to add new algorithms to offer more features is also limited by a fixed computing architecture. Automotive suppliers face significant challenges to develop a base computing platform that can be quickly modified and scaled to meet the cost and performance targets in entry level and high-end luxury vehicles around the world.

What are the current trends in ADAS design?

Traditionally for each ADAS functions there is an electronic control unit (ECUs)[6] which is not scalable and simple microcontrollers (MCUs) do not have the processing power to process the various sensor inputs from multiple radars, cameras, laser scanners, and ultra sonic sensors.



In order to develop a base computing platform that can be quickly modified and scaled to meet the cost and performance targets, traditionally an ASSP (Application specific standard product) is selected which has fixed input and output. Using ASSP, if suppliers want to support a wide range of vehicle models with single hardware architecture, they will have to design for the full set of ADAS features and scale back the feature offerings on the low end vehicles. ASSP has a fixed computing architecture. Often, the entire ASSP is consumed performing one specific algorithm, but in applications requiring multiple algorithms the processing functions need to be run in parallel.

In ASSP in order to handle the increased performance requirement, either the image resolution needs to be decreased or the frame rate reduced or multiple devices need to be used. Therefore ability to add new algorithms to offer more features is also limited by ASSP.

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FPGAs present an intriguing alternative to ADAS system design compared to fixed-function devices. FPGAs allow designers to customize the functionality and quickly change the I/O structures and hardware and data pipeline to be optimized for a particular algorithm.

How FPGA can benefit from these challenges and opportunities?

For the development of ADAS Systems, car makers require a common vehicle platform which can be reconfigured according to market needs since it saves the time-to-market and reduces cost of implementation while enhancing flexibility during manufacturing. FPGAs provide a suitable platform for developing the rapidly evolving ADAS Systems in automobiles.
Most important requirements of ADAS Includes

- Higher levels bandwidth and performance for processing video streams from multiple cameras
- Complex, real-time processing required to combine different sensor inputs
- Transmit, receive, and translate between multiple communication standards such as CAN, MOST, Ethernet, LVDS.

Meeting ADAS requirements

FPGAs provide an ideal platform for developing low-power, low-cost, high-performance, ADAS systems with the most favorable level of integration and flexibility.

FPGAs are reprogrammable. If there is any change in the processing architecture, it is possible to reprogram the hardware blocks in FPGA. Using FPGA, any changes can incorporate late in the design cycle. Using reprogrammable nature of FPGA, ADAS can support mutually exclusive functions using same FPGA.

FPGAs are well suited to meet the various processing requirements of an ADAS. Two or more distinctly different processes can be run in parallel on a single FPGA. The features like Rear View Camera , Rear cross path etc can be implemented through video processing, manipulation and graphics rendering while the feature effective Pedestrian Detection is performed through image processing analytics .

Another feature of FPGAs is device scalability. To add a new functionality to a serial DSP or an ASSP based system, it requires a complete re-architecture of the software design, even after moving to a more powerful device in the family. But in the case of an FPGA-based implementation, a new functional block can be added, utilizing previously unused FPGA logic and keeping the existing blocks as it is.

Figure 4 shows how the camera signal is split between the video- and image processing functions[2]. The raw processing power needed to perform these functions can quickly exceed that is available in a serial digital signal processor (DSP). Parallel processing along with hardware acceleration is a viable solution.

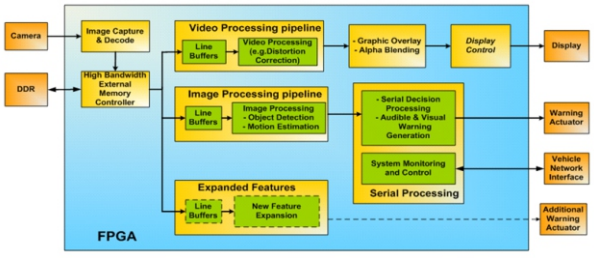

Figure 4:Camera based ADAS using FPGA

Camera-based ADAS applications require significant external memory access bandwidth especially in multi-camera systems. The data rate needed to store and access the images in external memory is usually high. Camera-based DA applications are memory bandwidth-intensive. These systems also commonly require memory controllers. FPGAs offer flexibility to add memory controllers in a cost effective manner. High end FPGAs offer memory controller blocks (MCBs) that designer can configure for 4, 8 or 16-

Advanced Driver Assistance System using FPGA

bit DDR, DDR2, DDR3, or LPDDR memory interfaces.

For processing streaming video or analyzing blocks of image data in camera-based DA systems, on-chip memory resources (block RAM, FIFO) that serve as line buffers are available in FPGA. Bayer transform, lens distortion correction, and optical-flow motion-analysis are examples of functions that require video line buffering.

Limitation of camera based ADAS System is the operating range of camera sensor is fairly limited compared to the radar- and sonar-based systems. So we can go for sensor fusion techniques. Limitations of camera sensors can be overcome by sensor fusion. Operating range of sensors like radar is more compared to camera sensors. The advantages of different types of sensors can be made useful in the case of sensor fusion.

Figure 5 shows the block diagram of the implementation of a sensor fusion DA System on PSoC[6]. PSoC (Programmable SoC) is a combination of a hard processor system (HPS), and a programmable logic (FPGA logic). The combination of HPS and FPGA logic in PSoC dramatically increases performance for real-time ADAS applications. It also enables greater system integration for bundling multiple applications.

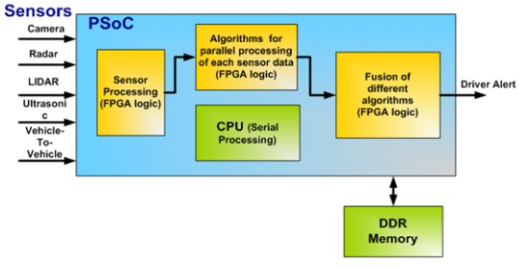

Figure 5: Sensor Fusion ADAS using PSoc

In order to process multiple algorithms simultaneously ADAS system designers are increasingly turning to FPGAs and PSoC to solve their challenging problems. Some low level sensor data processing benefits from parallel processing while some other high-level processing functions like system monitoring and control, decision making, warning generation etc are serial decision processes. FPGAs support both types of processing.

Benefits of FPGA based DA Systems compared to previous systems

❖ **Power:** The efficient implementation of data processing algorithm in FPGA reduces the power consumption compared to general-purpose computer architecture even though FPGAs consume considerable power generally.

❖ **Performance[2]:**

• Parallel processing of different functionalities can be easily achieved with FPGAs. It is difficult to run different processes simultaneously with an ASSP based design. But it is possible on a single FPGA.

• Functional partitioning of parallel and serial DA processes are possible. Functions that benefit from parallel processing are implemented in FPGA logic, while those more suited for serial processes are implemented in software. In FPGAs serial processes can be implemented either through Soft processors like Micro blaze (Xilinx) or through hard processors like ARM based Cortex –A9 processor.

• Reprogrammable nature is a major advantage of FPGA systems over the other systems. Reprogram ability is not possible with other alternatives.

• Device scalability: FPGAs are scalable and flexible to support a wide range of design requirements for ADAS applications. Designers can use a device that is priced and sized appropriately for the specified feature set.

Advanced Driver Assistance System using FPGA

• FPGAs meet external bandwidth requirements. FPGA memory controllers provide customized external memory interface design options to meet DA bandwidth needs and optimize all aspects of the cost equation.
• Availability of on chip memory resources like block RAMs.

• High-speed serial interfaces: Several FPGAs offer differential I/O that can operate at high speeds for the serial transport of data from external interfaces to the processing modules. It is possible to leverage these high-speed I/O capabilities along with the FPGA logic to implement emerging LVDS SerDes signaling protocols within the FPGA device itself, eliminating external components and reducing system cost.

❖ **Functional safety:** ADAS need to meet specific functional safety requirements. ISO26262 Quality certified FPGA devices, IP, Development tools, and FPGA design flow ensures functional safety of the DA System.

❖ **Better time to market[4]:** IP cores are readily available for various sensor processing applications especially for video and image processing. Because of the readily available quality certified IP Cores and FPGA device scalability, time to market for FPGA based DA systems are less compared to other alternatives.

❖ **Less cost of implementation:** Cost of implementation for FPGA based DA systems are less compared to others because of features like IP reuse, reprogram ability, device scalability, better integration or bundling of different features etc.

❖ **Product obsolescence:** While designing DA Systems, designers must consider life span of hardware components used. FPGA life cycles span up to 15 years which is longer than application-specific integrated circuits (ASICs) and ASSPs.

Issues that can impact FPGA selection

❖ **Firm-error immunity (7):** FPGAs depends on SRAM (static RAM) for configuration memory which makes them prone to neutron-induced errors which can cause thousands of failures in time .Moreover, these errors rise exponentially with fluctuations in temperature and altitude. But, Nonvolatile flash memory solutions do not suffer from neutron-induced errors and are therefore firm-error immune.

❖ **Electromagnetic interference (EMI):** EMI is a major concern in the case of FPGA selection also. But, in reprogrammable FPGAs, EMI can be quickly eliminated.

❖ **Speed**
ADAS applications require lightning-fast response times. FPGA response times are usually very low, may be several orders of magnitude faster than even a high-performance microcontroller. These fast response times help to reduce both EMI and power consumption.

Conclusion

Automatic driver assistance system (ADAS) is one of the fastest growing segments in automobile industry. In ADAS, sensors and algorithms are combined to understand the vehicle environment so that the driver can receive assistance or be warned of potential hazards. The processing platform requirements for an efficient ADAS system are architectural flexibility, platform scalability, external memory bandwidth, on-chip memory resources, high-speed serial interfaces, and parallel/serial process partitioning, functional safety. FPGA technology provides a suitable platform for such DA systems and is a viable alternative to standard ASSP and ASIC approaches.

Advanced Driver Assistance System using FPGA

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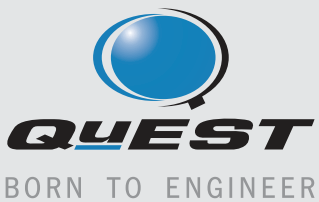

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